REMARKS

Claims 1-12, 14-23, and 25-93 are pending. Claims 32-93 are withdrawn from consideration. Independent claims 1, 18, 25, and 31 were rejected under 35 U.S.C. 103(a) as being obvious over Gosior (US 2003/0093655) in view of Sharma (5,841,663).

In the previous Office Action, the Examiner noted that dependent claims 13 and 24 would be allowable if rewritten to include any base and intervening claim limitations. Applicants respectfully maintained that the claims were patentable without any amendments, but to facilitate prosecution, the Applicants amended the independent claims 1, 18, 25, and 31 to include such limitations. The Examiner, however, has now entered new grounds for rejection. Independent claims 1 and 18 remain in amended form. Applicants are respectfully amending claims 25 and 31 to remove the previously added limitations, since the Applicants believe that the independent claims are allowable without any amendments.

Gosior describes a "single-chip embedded microprocessors having analog and digital electrical interfaces to external systems" [0001]. "Referring to FIG. 1, single-chip embedded processor 10 has input/output capabilities comprising a central eight thread processor core 12, clock input 14 with buffered output 16, various internal memory components shown as main RAM 18, a supervisory control unit (SCU) 20, peripheral adaptor 22 peripheral interface devices 24, an external memory interface 26 and a test port 28. The system is used for various embedded input/output applications such as baseband processor unit ("BBU") 30 connected to a RF transceiver 32 for communications applications and as an embedded device controller" [0022].

The Examiner argues that Gosior teaches implementing the processor on a programmable chip. However, notably absent in Gosior is any mention of programmable chips including Field Programmable Gate Arrays (FPGAs), Programmable Logic Devices (PLDs) or any other programmable devices. The only place Gosior uses the word programmable is with reference to Claim 1, when Gosior states "1. A programmable, single chip embedded processor system for input/output applications." However, claim 9 clarifies what is meant by programmable in Gosior by stating "wherein said controlling operating processor thread is programmable and comprises any of the available threads." Gosior is only describing a processor thread that is programmable, not any programmable chip. This is emphasized in the specification, when Gosior describes a "programming model for processor core 12" [0023], "two different threads executing programs

PAGE 13/15 * RCVD AT 5/16/2005 7:08:21 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/0 * DNIS:8729306 * CSID:5106630920 * DURATION (mm-ss):04-22

in different areas" [0036], and "executing eight independent programs on independent sets of data." [0044] A device having programmable threads is not inherently a programmable chip.

The single-chip in Gosior is in fact not a programmable chip. Gosior explicitly specifies that the single-chip is an ASIC. "As shown in FIG. 1 the system, as implemented as an application specific integrated circuit (ASIC), is contained within a box identified as processor 10." [0023] Additional language in Gosior further emphasizes that the single-chip is an ASIC. "The ASIC supports a multithread architecture with a shared memory model." [0028]

By contrast, the independent claims explicitly recite "configuring the processor core on the programmable chip" and "configuring the peripheral on the programmable chip." The single-chip ASIC in Gosior or any other ASIC for that matter does not have a processor core that can be configured or a peripheral that can be configured on a programmable chip. As noted on page 10, line 10 of the present application, "Some examples of programmable chips that can be implemented using the techniques of the present invention are programmable logic devices, complex programmable logic devices, programmable logic arrays, programmable array logic devices, and field-programmable gate arrays." Gosior does not describe any programmable chip and in fact describes only a nonprogrammable ASIC that can run different program threads.

The Examiner further argues that Gosior teaches parameter information for configuring a processor core and a peripheral. The Applicants respectfully disagree. The processor core and other components in Gosior are not parameterizable and are in fact fixed ASIC components. "A three port register RAM module 36 comprising eight sets of eight words is used for registers R0 to R7 for each of the eight processor threads. A boot ROM memory 38 can store several non-volatile programs and data including the system boot image and various application specific tables such as a code table for RF transceiver 32 applications." [0024] The ASIC includes "a sixteen-bit timer facility, referenced to master clock 14 for timing processor events or sequences." [0024] None of these components is ever said to be parameterizable in Gosior. The very fact that they are implemented on an ASIC argues that they are not parameterizable components.

As noted in the Background of the present application, "It has proven difficult to enable parameterization of processor cores and peripherals in a programmable chip. Differing standards for peripheral interface buses cause problems. Many problems occur at the interconnection level

PAGE 14/15 * RCVD AT 5/16/2005 7:08:21 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/0 * DNIS:8729306 * CSID:5106630920 * DURATION (mm-ss):04-22

between processor and peripherals." Consequently, the claims allow receiving parameter information, for example 16-bit or 32-bit for a processor core or 1200 baud or 2400 baud for a UART. Nothing in Gosior or any other reference cited by the Examiner teaches or suggest receiving parameter information to configure a processor core and a peripheral. Consequently, the independent claims 1, 18, 25, and 31 are believed allowable for at least these reasons.

In light of the above remarks relating to independent claims, the remaining dependent claims are believed allowable for at least the reasons noted above. Applicants believe that all pending claims are allowable and respectfully request a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

Respectfully submitted,
BEYER WEAVER & THOMAS, LLP

Godfrey K. Kwan
Reg. No. 46,850

P.O. Box 70250
Oakland, CA 94612-0250
(510) 663-1100

PAGE 15/15 * RCVD AT 5/16/2005 7:08:21 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/0 * DNIS:8729306 * CSID:5106630920 * DURATION (mm-ss):04-22